REMARKS

Claims 1-16 are pending in this Application, by this Amendment, Figures 1-3 and the Title of the Invention are amended to better conform with formalities suggested by the Office Action. Claims 3, 15 and 16 is also amended. No new matter is added. Applicant appreciates the Examiner's admission of allowable subject matter in claims 4 and 5. However, Applicant asserts that all of the claims are directed to patentable subject matter for the reasons set forth below.

The Office Action objects to FIGS. 1-3 under 37 C.F.R. §1.121(d) due to minor informalities. By this Amendment, FIGS. 1-3 are amended as suggested by the Office Action. Accordingly, withdrawal of the objection is respectfully requested.

The Office Action also objects to the Title of the Invention. By this Amendment, the Title of the Invention is amended as suggested by the Office Action. Accordingly, withdrawal of the objection is respectfully requested.

The Office Action also objects to the Specification stating that the Specification does not provide the appropriate antecedent basis for the claimed subject matter in claims 2-3 and 15. The Office Action further rejects claims 2-3 and 15 under 35 U.S.C. § 112, first paragraph, due to the same misunderstanding of what the Specification describes. The objection and rejection are respectfully traversed for the reasons put forth below.

In particular, Applicants assert that an example of a type of a multiplexer is disclosed in the present application in FIGS. 5 and 6 which, when reviewed in light of the relevant text in the Detailed Description and the knowledge of one of ordinary skill in the art, provides an adequate antecedent basis for the claimed subject matter as well as the necessary support under 35 U.S.C. § 112, first paragraph.

Applicant first notes the Office Action's statement on page 4 that "*Applicant's multiplexer has only 2* ***unique*** *inputs (FRP and the delayed PCLK) and therefore cannot properly function as a typical multiplexer*" {bolded emphasis added}. While the Office Action is partially correct in that multiplexers generally have at least two inputs, there is no requirement that

such inputs must be independent of one another. To that end, Applicant points out that a signal and a delayed version of the same signal, such as the PCLK, PCLK' and FRP signals of FIGS. 5 and 6, can be combined by a multiplexer even if details describing their inter-relationship are not shown in Figure 5.

Applicant next notes the Office Action's statement on page 4 that a "*multiplexer in the communication arts* ***combines*** *multiple inputs to create a single output*" {bolded emphasis in original} to which the Applicant respectfully points out that the circuitry in FIG. 6 conforms with the broad definition of a multiplexer in that it combines the FRP signal (which happens to be a delayed version of PCLK) with PCLK' (which happens to be a delayed version of PCLK with a different delay period) using the NAND gate 640 and inverter 650 to create a single output, i.e., the SRP signal. Thus, it should be appreciated that, in the present circumstance where inputs are related/interdependent, certain standard gates, such as NAND gates or NOR gates, can adequately perform the appropriate multiplexing/combining functions.

Accordingly, while the term "multiplexer" does not precisely fit either of the two specific definitions provided by the Office Action, the term "multiplexer" is nonetheless descriptive of the underlying processes ongoing in FIGS. 5-6 and not repugnant to the broad meaning of the term. Thus, withdrawal of both the objection and rejection is respectfully requested.

The Office Action further rejects claim 3 under 35 U.S.C. §112, second paragraph. By this Amendment, claim 3 is amended to obviate the rejection. Accordingly, withdrawal of the rejection is respectfully requested.

The Office Action further rejects claims 10-11 under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

In particular, Applicant respectfully asserts that, contrary to the assertions of the Office Action on page 7 that the language of claim 10 must infer "*a singular clock*", an appropriate construction of the phrase "wherein the first control signal and the second control signal are driven by a clock signal" (from claim 10) can merely require that the first control signal and the second control signal be driven by at least one common clock signal. Accordingly, while the Office Action protests that "*the first and second control signals are*

actually driven by two separate internal clock signals (FRP and SRP respectfully)", the language of claim 10 is permissive of this as long as the first and second control signals are driven using at least one common clock. Note that in the example of FIG. 6, FRP is derived from PCLK, and SRP is derived from both PCLK and PCLK' (which happens to be a delayed version of PCLK). Accordingly, FRP and SRP are both derived from PCLK, which is entirely consistent with the language of "*[a] first control signal and [a] second control signal ... driven by a clock signal.*" Accordingly, withdrawal of the rejection is respectfully requested.

The Office Action reject rejects claims 1 and 6-14 under 35 U.S.C. §103(a) over Applicant's "Description of Related Art" (DRA) in view of Lee (U.S. Patent No. 6,564,287); rejects claims 2-3 and 15 under 35 U.S.C. §103(a) over Applicant's in view of Lee and Paul (U.S. Patent No. 6,629,226); and rejects claim 16 under 35 U.S.C. §103(a) over Applicant's in view of Lee and Shinozaki (U.S. Patent No. 6,084,802). These rejections are respectfully traversed.

In particular, Applicant asserts that it would not have been obvious at the time of the invention to one of ordinary skill in the art to modify the DRA using the teachings of Lee, Paul and Shinozaki, individually or in combination, to teach or suggest a pipeline memory device that includes a data fetching control circuit that is configured to generate a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal ...a first pipeline stage that latches the data on the data transfer path in response to the first pipeline control signal and a second pipeline stage that latches the data latched by the first pipeline stage in response to the second pipeline control signal, as recited in independent claim 1 and similarly recited in independent claim 6.

The DRA discloses an exemplary block diagram of a memory device 10 with a pipeline configuration. In operation, the pipeline memory device 10 receives an address signal ADD through the address buffer 12 and the address register 14. The received address signal ADD then addresses the

memory cell 21 by the row decoder 18 and the column decoder 20 via the address pre-decoder 16. In response to a clock signal CLK and a command signal CMD, the synchronous control circuit 15 can generate a first pipeline control signal FRP, a second pipeline control signal SRP, and a data output clock signal (CLKDQ). See, par. 4-6. The DRA does not teach or suggest a data fetching control circuit that is configured to generate a first pipeline control signal, in response to a first clock signal ... and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal, [wherein the] second pipeline stage latches the data latched by the first pipeline stage in response to the second pipeline control signal, an issue admitted by the Office Action admits on pages 8-9.

Lee discloses a semiconductor memory device having a fixed CAS and RAS latency. See, Abstract. Figure 1 of Lee shows a memory device having a sense amplifier 20, a pipeline circuit 30 and a data output driver 34. Figure 3 of Lee discloses details of a pipeline control signal generation circuit 28 used to control the pipeline circuit 30 of Figure 1.

As shown in Figure 3, a clock signal CLK is used to generate two clock signals, PCLK and p3 via buffers 50 and 52. The PCLK clock signal is then used to generate control signal p1, and clock signal p3 is used to generate a clock signal p2. However, the Office Action has not shown that Lee teaches or suggests a data fetching control circuit that is configured to generate a first pipeline control signal, in response to a first clock signal ... and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal [wherein the] second pipeline stage latches the data latched by the first pipeline stage in response to the second pipeline control signal.

To the contrary, while the Office Action is correct in stating that clock signal p2 is created in response to clock signal p3, signal p3 cannot be equated to a "first pipeline control signal" as it apparently is not used to latch data in a first pipeline stage from which the second pipeline stage (controlled by signal p2) receives data.

Applicant respectfully points out that the Office Action's analogy of p3 to a "first pipeline control signal" is in error. As clearly shown in Figure 4, which depicts details of the pipeline device 30 of Figure 1, clock signal p3 is used to control a third pipeline stage 64 that receives data latched by the second pipeline stage 62. In order for the Office Action's construction to be correct, pipeline stage 64 would need to feed data to pipeline stage 62, **which is clearly the opposite of the present situation**. Thus, the Office Action has failed to show that Lee provides for the deficiencies of the DRA.

Paul and Shinozaki do not disclose a data fetching control circuit that is configured to generate a first pipeline control signal, in response to a first clock signal ... and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal ... wherein a first pipeline stage that latches the data on the data transfer path in response to the first pipeline control signal and a second pipeline stage that latches the data latched by the first pipeline stage in response to the second pipeline control signal, nor does the Office Action make such an assertion. Thus, Paul and Shinozaki do not provide for the apparent deficiencies of Lee and the DRA.

The Office Action has not established a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations, there must be some motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the reference teachings and there must be a reasonable likelihood of success to combine the references. See MPEP §2143, for example.

As discussed above, none of the applied art of record, individually or in combination, teaches or suggests all the claim limitations.

Further, the Office Action has failed to provide a requisite motivation as to why one of ordinary skill in the art would be motivated to modify the memory disclosed in the DRA to use the control signal generation circuit of Lee. While the Office Action asserts that "*it would have been obvious to a person of ordinary skill in the art ... [because] doing so would have been to provide variable operational modes of latency and variable operation modes*

of burst lengths, thus increasing system flexibility and improving performance", this assertion is problematic for a number of reasons.

First, the assertion does not appear in any of the cited art of record.

Second, by using clock signal p3 (as suggested by the Office Action) to control a first pipeline stage in the memory device of the DRA, there is no indication that the modified memory device would even be operable, much less exhibit improved performance and flexibility.

Thus, the independent claims are directed to patentable subject matter, and the dependent claims are directed to patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections under 35 U.S.C. §103(a) is respectfully requested.

In the event that there are any outstanding matters remaining in the present application, please contact B. Y. Mathis (Reg. No. 44,907) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,
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Attached: Replacement Sheets for Figures 1-3

In the Figures

Please replace Figures 1-3 using the replacement sheets attached hereto.